HT82V863R
CCD Digital Signal Processor

Features

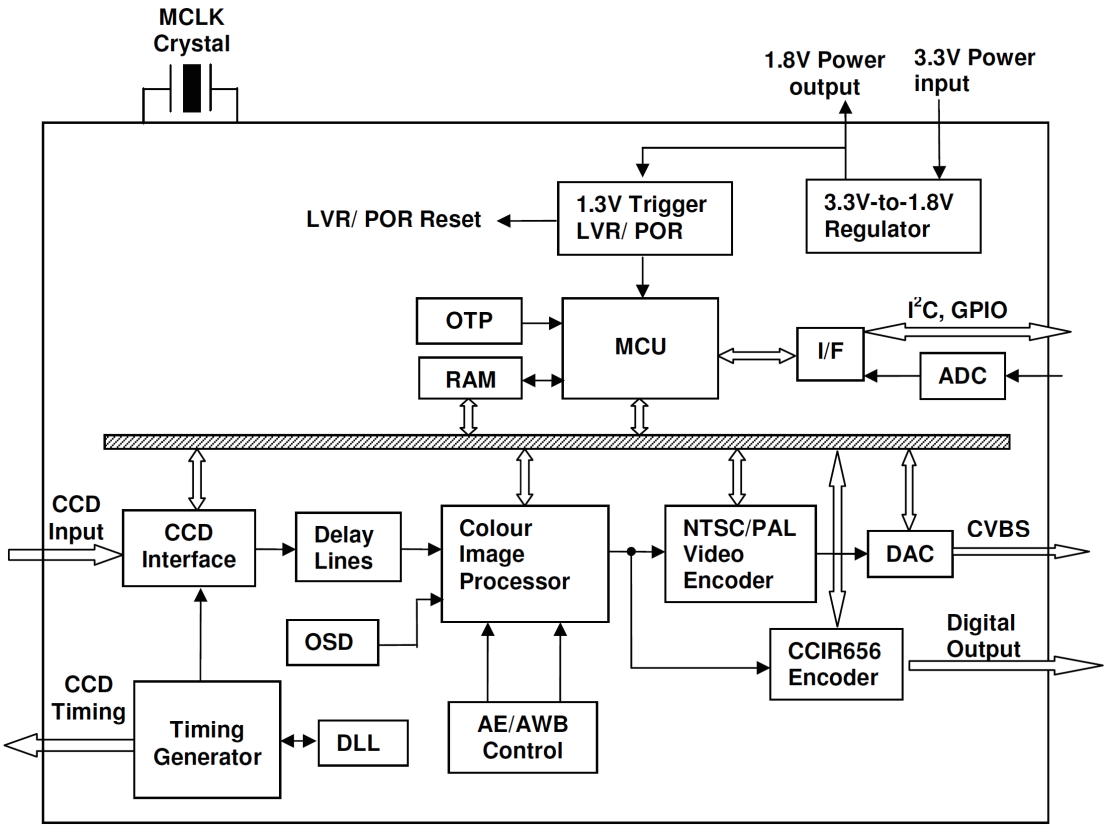
- Input: Supports Ye, Mg, Cy, G colour filters for NTSC/PAL, 270K/320K/410K/470K CCD sensors
- Output: NTSC/PAL Analog CVBS
- Automatic CCD Defect compensation
  Up to 50 bad pixels and 4 consequential bad pixels correction
- Automatic Back Light compensation
- Programmable False Colour suppression
- Programmable High Light suppression
- Programmable Sharpness enhancement
- Programmable Colour Saturation and Hue function
- Programmable Contrast and Brightness function
- Programmable GAMMA curve
- Integrate a 96-step CCD timing generator
- Support AE/AWB algorithm function
- Support OSD function
- Integrate a 2-D DNR function
- Integrate the digital WDR
- Integrate the digital Line Lock function to reduce colour rolling
- Integrate a NTSC/PAL video encoder
- Integrate a 10-bit DAC
- Support CCIR656 digital out
- Integrate a one-channel 6-bit ADC
- Integrate OTP ROM with ISP function for multiple programming codes
- Support Mirror function
- Support a master I^2C interface for external EEPROM to store parameters
- Support a slave I^2C interface for communication with an external host
- Embedded LVR and POR circuits
- Embedded 3.3V-to-1.8V regulator
- Single 3.3V power supply
- 64/80-LQFP package

General Description

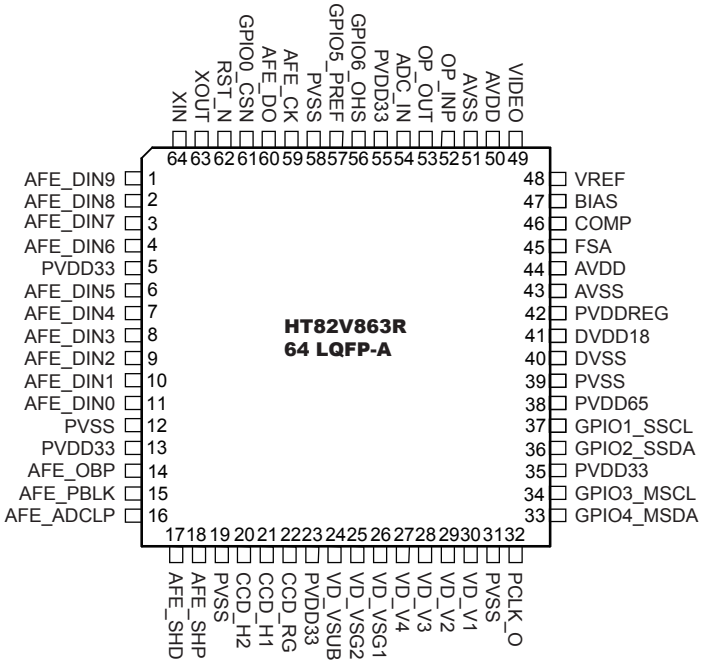
The HT82V863R is a single chip digital image processor for Ye, Cy, Mg and G colour CCD video camera systems. It receives CFA patterns from colour CCDs and generates NTSC/PAL CVBS signals using internal video encoders and the 10-bit DAC. In addition, it also provides an AE/AWB algorithm, timing generation module together with other circuitry.

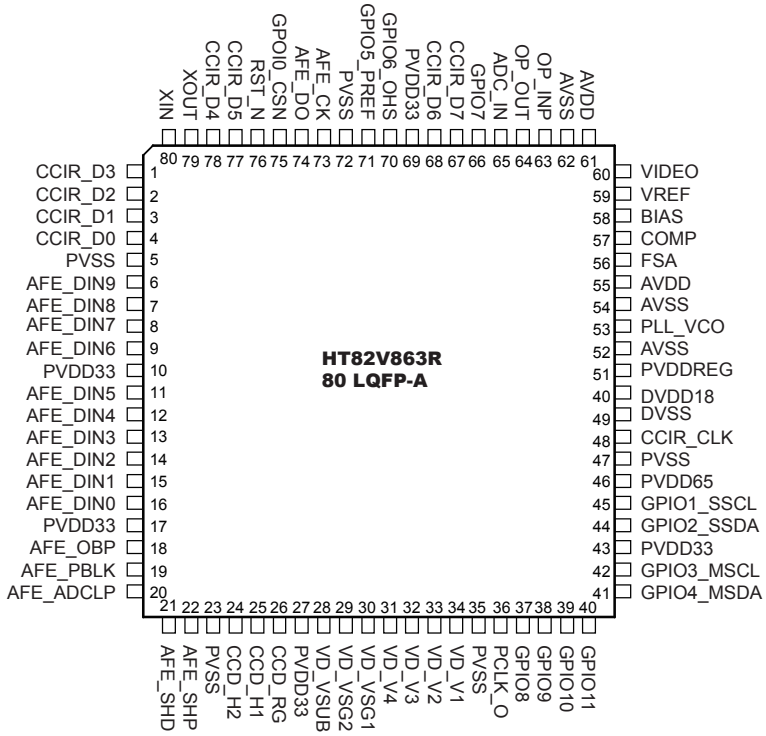
The device contains a microcontroller in which an OTP ROM is integrated internally to implement the basic camera functions such as the AE/AWB algorithm. The video camera system consists of a CDS/AGC/ADC IC (HT82V842A), DSP IC (HT82V863R), Vertical Driver IC (HT82V805) and CCD sensors. It also provides a proprietary function to eliminate so called “line crawl” and automatic CCD defect compensation function to correct up to 30 bad pixels and 4 consequential bad pixels.

Block Diagram



Pin Assignment





Pin Description

Pin					Description
Name	DIR	TYP	PUL	mA	
CCIR_D3	O	—	—	4	CCIR656 Encoder Data Output bit 3
CCIR_D2	O	—	—	4	CCIR656 Encoder Data Output bit 2
CCIR_D1	O	—	—	4	CCIR656 Encoder Data Output bit 1
CCIR_D0	O	—	—	4	CCIR656 Encoder Data Output bit 0
PVSS	—	P	—	—	Pad ground pin
AFE_DIN9	I	—	—	—	CCD Data input bit 9
AFE_DIN8	I	—	—	—	CCD Data input bit 8
AFE_DIN7	I	—	—	—	CCD Data input bit 7
AFE_DIN6	I	—	—	—	CCD Data input bit 6
PVDD33	—	P	—	—	3.3V pad power pin
AFE_DIN5	I	—	—	—	CCD Data input bit 5
AFE_DIN4	I	—	—	—	CCD Data input bit 4
AFE_DIN3	I	—	—	—	CCD Data input bit 3
AFE_DIN2	I	—	—	—	CCD Data input bit 2
AFE_DIN1	I	—	—	—	CCD Data input bit 1
AFE_DIN0	I	—	—	—	CCD Data input bit 0
PVSS	—	P	—	—	Pad ground pin
PVDD33	—	P	—	—	3.3V pad power pin
AFE_OBP	O	—	—	4	Clamp pulse output for optical black function
AFE_PBLK	O	—	—	4	Blanking pulse output for AFE
AFE_ADCLP	O	—	—	4	Clamp pulse output for AFE
AFE_SHD	O	—	—	4	Sample hold pulse output for data
AFE_SHP	O	—	—	4	Sample hold pulse output for reference
PVSS	—	P	—	—	Pad ground pin
CCD_H2	O	—	—	12	Horizontal shift register Clock 2 for CCD
CCD_H1	O	—	—	12	Horizontal shift register Clock 1 for CCD
CCD_RG	O	—	—	12	Reset pulse output for CCD
PVDD33	—	P	—	—	3.3V pad power pin
VD_VSUB	O	—	—	4	CCD substrate bias pulse output for Vertical Driver
VD_VSG2	O	—	—	4	Readout pulse 2 for Vertical Driver
VD_VSG1	O	—	—	4	Readout pulse 1 for Vertical Driver
VD_V4	O	—	—	4	Vertical shift register clock 4 for Vertical Driver
VD_V3	O	—	—	4	Vertical shift register clock 3 for Vertical Driver
VD_V2	O	—	—	4	Vertical shift register clock 2 for Vertical Driver
VD_V1	O	—	—	4	Vertical shift register clock 1 for Vertical Driver
PVSS	—	P	—	—	Pad ground pin
PCLK_O	O	—	—	12	Pixel Clock Output
GPIO8	B	—	U	4	GPIO [8] or PWM [3] output
GPIO9	B	—	U	4	GPIO [9] or UART Receiver data input, RXD.
GPIO10	B	—	U	4	GPIO [10]
GPIO11	B	—	U	4	GPIO [11]
GPIO4_MSDA	B	—	U	4	GPIO [4] or Master mode I^2C Data Input/Output
GPIO3_MSCL	B	—	U	4	GPIO [3] or Master mode I^2C Clock Output
PVDD33	—	P	—	—	3.3V pad power pin
GPIO2_SSDA	B	—	U	4	GPIO [2] or Slave mode I^2C Data Input/Output
GPIO1_SSCL	B	—	U	4	GPIO [1] or Slaver mode I^2C Clock Input

Pin					Description
Name	DIR	TYP	PUL	mA	
PVDD65	—	P	—	—	6.5V pad power pin
PVSS	—	P	—	—	Pad ground pin
CCIR_CLK	O	—	—	12	CCIR656 Encoder Clock Output
DVSS	—	P	—	—	Digital ground pin
DVDD18	—	P	—	—	1.8V digital power pin
PVDDREG	—	P	—	—	3.3V regulator power pin
AVSS	—	P	—	—	OP, DAC and Regulator Ground pin.
PLL_VCO	AO	—	—	—	PLL VCO Output
AVSS	—	P	—	—	OP, DAC and Regulator Ground pin
AVDD	—	P	—	—	3.3V OP and DAC Power pin
FSA	AO	—	—	—	DAC Full-Scale Adjust Control
COMP	AO	—	—	—	DAC Compensation pin
BIAS	AO	—	—	—	DAC Current Source Bias Pin
VREF	AI	—	—	—	DAC Bandgap Reference Voltage Output
VIDEO	AO	—	—	—	DAC VIDEO Output
AVDD	—	P	—	—	3.3V OP and DAC Power pin
AVSS	—	P	—	—	OP and DAC Ground pin
OP_INP	AI	—	—	—	OP Buffer Positive Input
OP_OUT	AO	—	—	—	OP Buffer Output
ADC_IN	AI	—	—	—	A/D Converter Analog Input
GPIO7	B	—	U	—	GPIO [7] or 27MHz Clock input
CCIR_D7	O	—	—	4	CCIR656 Encoder Data Output bit 7
CCIR_D6	O	—	—	4	CCIR656 Encoder Data Output bit 6
PVDD33	—	P	—	—	3.3V pad power pin
GPIO6_OHS	B	—	U	4	GPIO [6] or PWM [2] output or UART Transmitter data output, TXD, or Digital Video HSYNC Output.
GPIO5_PREF	B	—	U	4	GPIO [5] or PWM [1] output or Power Line Reference Clock Input
PVSS	—	P	—	—	Pad ground pin
AFE_CK	O	—	—	4	SPI Clock Output for AFE
AFE_DO	O	—	—	4	SPI Data Output for AFE
GPIO0_CSN	B	—	U	4	GPIO[0] or PWM[0] output or UART Transmitter data output, TXD, or SPI Chip Enable Output for AFE
RST_N	I	S	—	—	System Reset, Active Low
CCIR_D5	O	—	—	4	CCIR656 Encoder Data Output bit 5
CCIR_D4	O	—	—	4	CCIR656 Encoder Data Output bit 4
XOUT	O	—	—	—	Oscillator output
XIN	I	—	—	—	Oscillator input for MCLK

Note: DIR: pin direction, B: bi-directional, O: output, I: input
AI: Analog input, AO: Analog output, TYP: pin type
T: tri-state, OD: open-drain, S: Schmitt trigger, P: Power pin
PUL: pin internal pull up/down 75Ω resistor
U: pull-up, D: pull-down, mA: pin driving current capability

Absolute Maximum Ratings

Power Supply Voltage V_{CC} ..... -0.3V~4.3V
Input Voltage V_{IN} ..... -0.3V~V_{CC}+0.3V
Output Voltage V_{out} ..... -0.3V~V_{CC}+0.3V
Storage Temperature T_{STG} ..... -40°C~150°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power supply	3.0	3.3	3.6	V
V_{IN}	Input voltage	0	—	V_{CC}	V
T_{OP}	Operating temperature	-20	25	70	°C
f_{CK}	Input clock frequency	—	28.7	—	MHz

D.C. Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	—	—	—	0.8	V
V_{IH}	Input high voltage	—	2.0	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V
V_{OH}	Output high voltage	—	2.4	—	—	V
I_{DD}	Operating current	—	—	80	—	mA
V_{T-}	Schmitt trigger input low voltage	—	0.8	1.1	—	V
V_{T+}	Schmitt trigger input high voltage	—	—	1.6	2.0	V
R_I	Input pull-up/pull-down resistance	V_{IL}=0V or V_{IH}=Vcc	—	75	—	Ω

A.C. Characteristics

Clock Characteristics

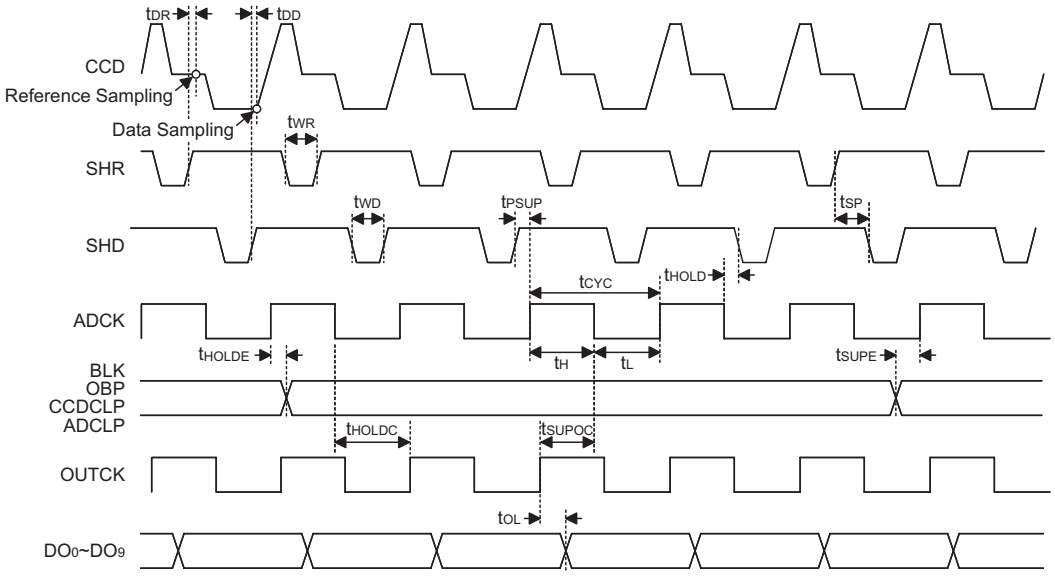
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CK}	Oscillator Clock Frequency	-500ppm	28.7	+500ppm	MHz
D_{CK}	Oscillator Clock Duty Cycle	45	50	55	%

Reset Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RST_N}	External System Reset pulse width	—	1	—	ms

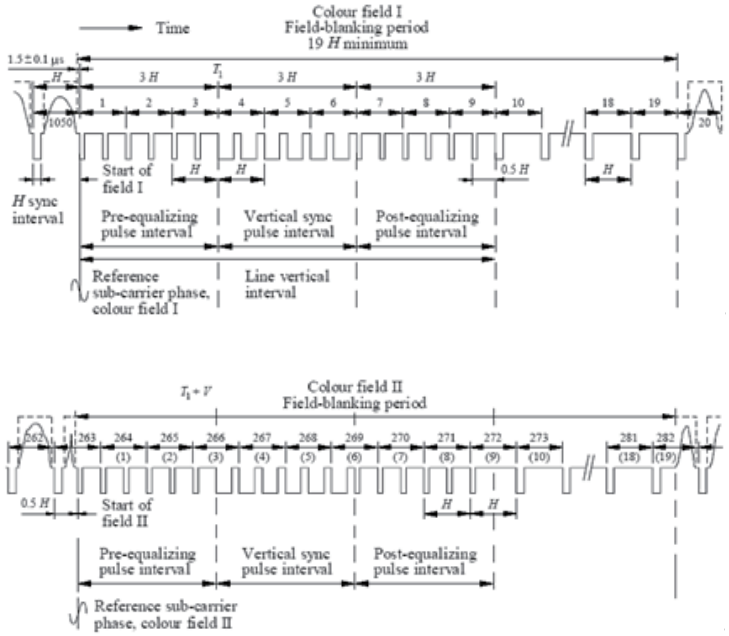
CCD Input Interface Timing

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_S	Conversion Frequency	3.0V	—	0.5	—	20	MHz
t_{CYC}	Clock Cycle Time	3.0V	—	50	—	—	ns
t_R	Clock Rising Time	3.0V	—	—	—	2	ns
t_F	Clock Falling Time	3.0V	—	—	—	2	ns
t_L	Clock Low Period	3.0V	—	23	—	—	ns
t_H	Clock High Period	3.0V	—	23	—	—	ns
t_{WR}	SHR Pulse Width	3.0V	—	11	—	—	ns
t_{WD}	SHD Pulse Widh	3.0V	—	11	—	—	ns
t_{DR}	SHR Sampling Aperture	3.0V	—	—	—	4	ns
t_{DD}	SHD Sampling Aperture	3.0V	—	—	—	4	ns
t_{PSUP}	Data Pulse Setup	3.0V	—	2	—	—	ns
t_{HOLD}	Data Pulse Hold	3.0V	—	5	—	—	ns
t_{SP}	Sampling Pulse Non-overlay	3.0V	—	1	—	—	ns
t_{SUPE}	Enable Pulse Setup	3.0V	—	10	—	—	ns
t_{HOLDE}	Enable Pulse Hold	3.0V	—	10	—	—	ns
t_{SUPOC}	OUTCK Setup	3.0V	—	0	—	—	ns
t_{HOLDC}	OUTCK Hold	3.0V	—	10	—	—	ns
t_{DLD}	3-state Disable Delay	3.0V	Active→High-Z	—	20	—	ns
t_{DLE}	3-state Disable Delay	3.0V	High-Z→Active	—	20	—	ns
t_{OL}	ADC Output Data Delay	3.0V	—	—	18	—	ns

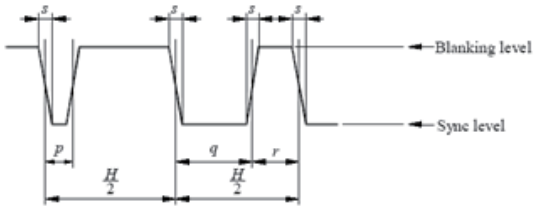


Note: Normally, the AFE ASIC registers are set to ignore OUTCK, and only use ADCK.

TV Encoder Output Interface Timing



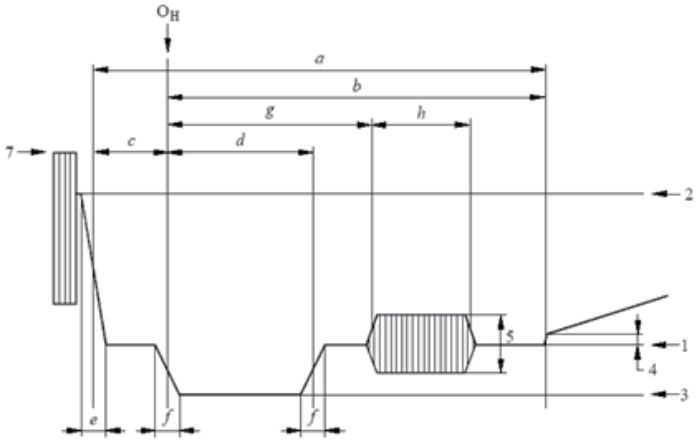
NTSC Vertical Timing



Equalizing Pulse and Sync Pulse Interval Timing

Table equalizing pulse and sync pulse interval timing.

Symbol	Characteristics(μs)	NTSC	PAL
p	Duration of equalizing pulse	2.3±0.1	2.35±0.1
q	Duration of field-synchronizing pulse	27.1	27.3
r	Interval between field-synchronizing pulse	4.7±0.1	4.7±0.2
s	Build-up timing (10 to 90%)	≤0.25	0.2±0.1



Details of Line Synchronizing Signal

Table Details of line synchronizing signal.

Symbol	Characteristics (μs)	NTSC	PAL
d	Synchronizing pulse	4.7±0.1	4.7±0.2
e	Build-up time of the line-blanking pulse	≤0.48	0.3±0.1
f	Build-up time of the line-synchronizing pulse	≤0.25	0.2±0.1
b	Line-blanking interval	9.2~10.3	12±0.2
c	Front porch	1.27~2.22	1.5±0.3
g	Start of sub-carrier burst	4.71~5.71	5.6±0.1
h	Duration of sub-carrier burst	2.23~3.11(9±1 cycles)	2.25±0.23(10±1 cycles)
H	Nominal line period	63.5555	64

CCIR656 Encoder Interface Timing

The CCIR656 Encoder connects to the digital component video signals using 525 lines for NTSC systems or 625 lines for PAL systems.

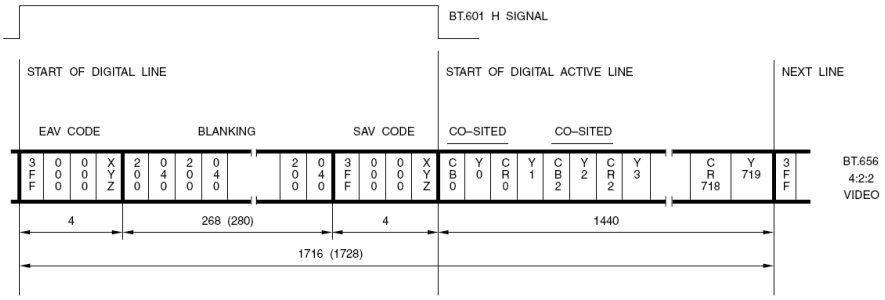
The data stream is a sequence of 8-bit bytes, transmitted at a rate of 27 MBbyte/s. The video pixel data horizontal scan lines are delimited in the stream using 4-byte long SAV (Start of Active Video) and EAV (End of Active Video) code sequences.

Individual pixels in a line are coded in YCbCr “4:2:2” format. After an SAV code (4 bytes) is sent, the first 8 bits of Cb (chroma U) data are sent and then 8-bit data of Y (luma), followed by 8-bit data of Cr (chroma V) for the next pixel and then 8 bits of Y.

TV System		PAL (625 lines)	NTSC (525 lines)
V-digital field blanking			
Field 1	Start (V=1)	Line 624	Line 1
	Finish (V=0)	Line 23	Line 10
Field 2	Start (V=1)	Line 311	Line 264
	Finish (V=0)	Line 336	Line 273
F-digital field identification			
Field 1	F=0	Line 1	Line 4
Field 2	F=1	Line 313	Line 266

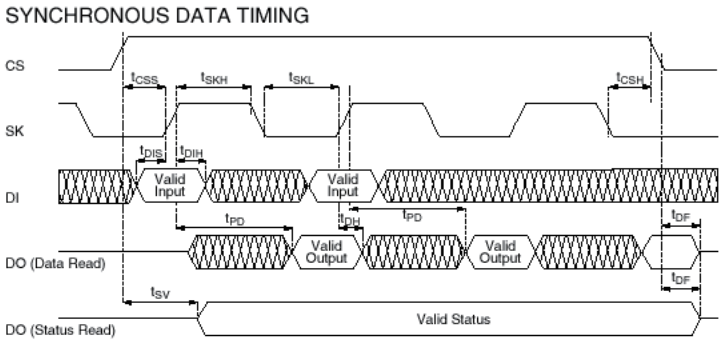
Video DatField-Blanking Definition

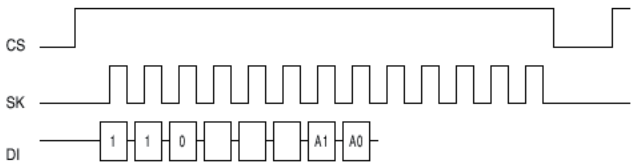
Horizontal Timing



One Scan Line Parallel Interface Data

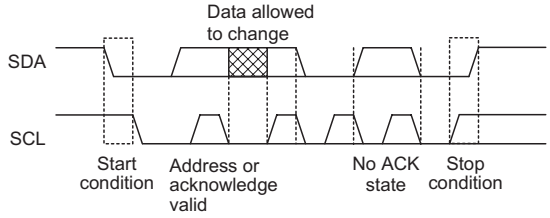
SPI Interface Timing

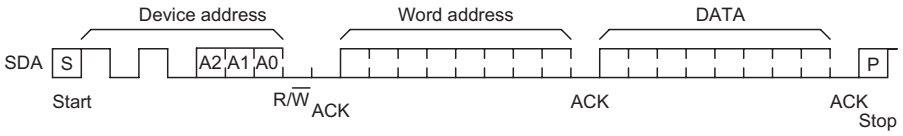




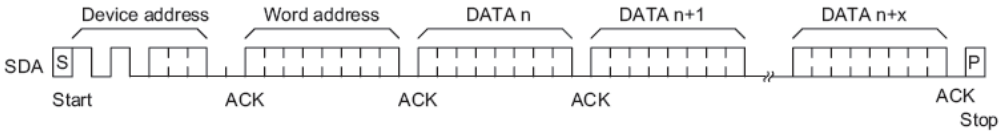
Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SK}	SK Clock Frequency	—	0	250	kHz
f_{SKH}	SK High Time	—	1	—	μs
f_{SKL}	SK Low Time	—	1	—	μs
t_{CS}	Minimum CS Low Time	—	1	—	μs
t_{CSS}	CS Setup Time	—	0.2	—	μs
t_{DH}	DO Hold Time	—	70	—	ns
t_{DIS}	DI Setup Time	—	0.4	—	μs
t_{CSH}	CS Hold Time	—	0	—	ns
t_{DIH}	DI Hold Time	—	0.4	—	μs
t_{PD}	Output Delay	—	—	2	μs
t_{SV}	CS to Status Valid	—	—	1	μs
t_{DF}	CS to DO in Hi-Z	$CS=V_{IL}$	—	0.4	μs
t_{WP}	Write Cycle Time	—	—	15	ms

I²C Interface Timing

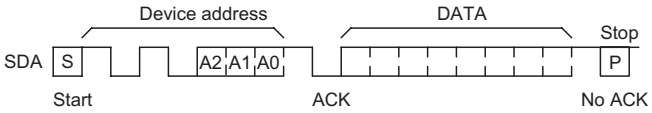




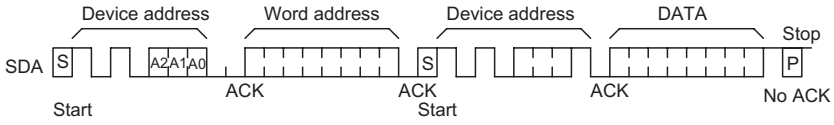
Byte Write Timing



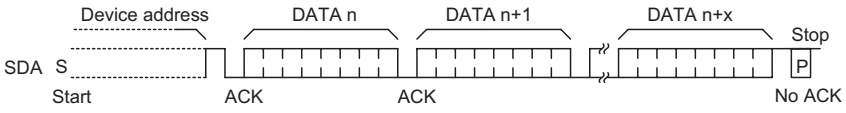
Page Write Timing



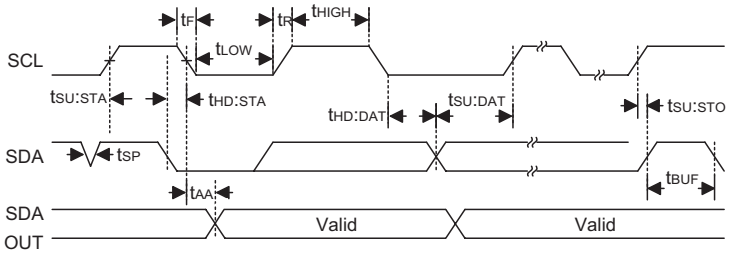
Current Read Timing



Random Read Timing

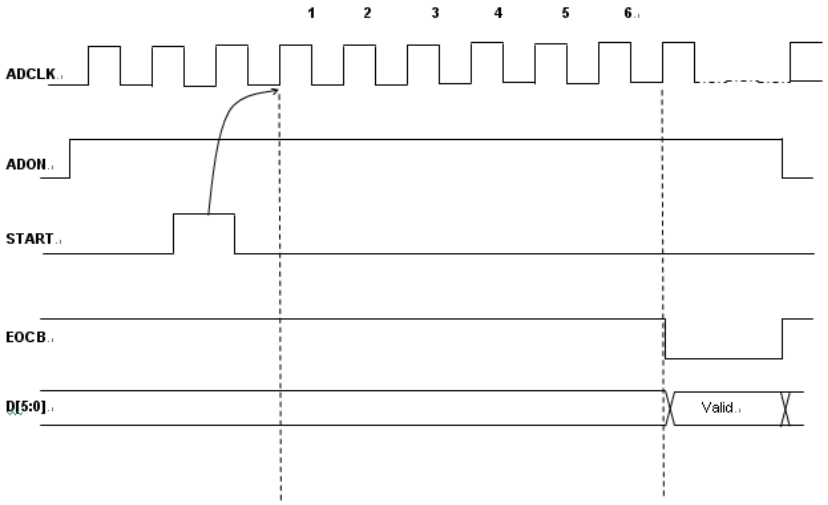


Sequential Read Timing



Symbol	Parameter	Remark	Standard Mode*		V_{CC}=5V±10%		Unit
			Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	—	—	100	—	400	kHz
t_{HIGH}	Clock High Time	—	4000	—	600	—	ns
t_{LOW}	Clock Low Time	—	4700	—	1200	—	ns
t_R	SDA and SCL Rise Time	Note	—	1000	—	300	ns
t_F	SDA and SCL Fall Time	Note	—	300	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	4000	—	600	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	4000	—	600	—	ns
$t_{HD:DAT}$	Data Iuput Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Iuput Setup Time	—	200	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	4000	—	600	—	ns
t_{AA}	Output Valid from Clock	—	—	3500	—	900	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4700	—	1200	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	—	5	ms

A/D Converter Interface Timing



Functional Description

CCD Interface

The CCD interface is used to capture the image and receive the CMYG CFA CCD raw data and the control signals generated from the analog front-end module. Then the CCD raw data together with the control signals will be correctly manipulated such as for black clamp operation, bad pixel compensation, etc. The processed raw data and control signals will be eventually sent to the Colour Image Processor to perform further image signal manipulations.

Colour Image Processor

The heart of the surveillance camera is the Colour Image Processor in which the raw data derived from the CCD interface is processed. In addition to the colour mosaic interpolation, several colour image processor main functions include the edge extraction and enhancement, colour correction, auto exposure support and white balance, colour space transform, gamma correction and false colour suppression.

Timing Generator

This is a programmable 96-step precision timing generator embedded with a DLL to perform timing fine tuning and to generate all the CCD data related control timings.

TV Encoder

This provides a 10-bit YCbCr digital input interface to accept the data stream sent from the Colour Image Processor (or equivalent circuitry) and to convert the data into the NTSC or PAL TV composite signal or Y/C signal.

Line Lock

A Line-Lock function is available on most CCTV cameras and is used to prevent picture colour rolling on the monitor, which results from the difference between the surveillance camera exposure frequency and the AC power line frequency. Colour rolling will cause a vital picture information loss and will be irritating for the viewer.

A/D Converter

The device provides a 6-bit A/D Converter.

OSD Generator

The device can generate up to 4 lines with a maximum of 16 characters, each of which can be up to 16×16 font size. The scaling factor can be up to 8 times on both the horizontal direction and vertical direction.

Back Light Compensation – BLC

The Back Light Compensation will provide perfect exposure for an object in front of very strong back light, no matter whether the main object is moving toward the center, upper, lower, left, right part or any location in the screen. The HT82V863R device provides a smart adaptive BLC algorithm to perform compensation, followed by the exposure level, with a fast speed so that no matter where on the screen the main object is moving to, it always provides a clear picture.

DWDR

Digital WDR is a proprietary algorithm to provide clear images even under back light circumstances where there are both very bright and very dark areas simultaneously in the view of the camera. In short, DWDR allows the viewer to see details in both areas.

CCIR656 Encoder

The CCIR656 Encoder accepts the data stream derived from the Colour Image Processor and converts the data into ITU_R BT656 digital output signals.

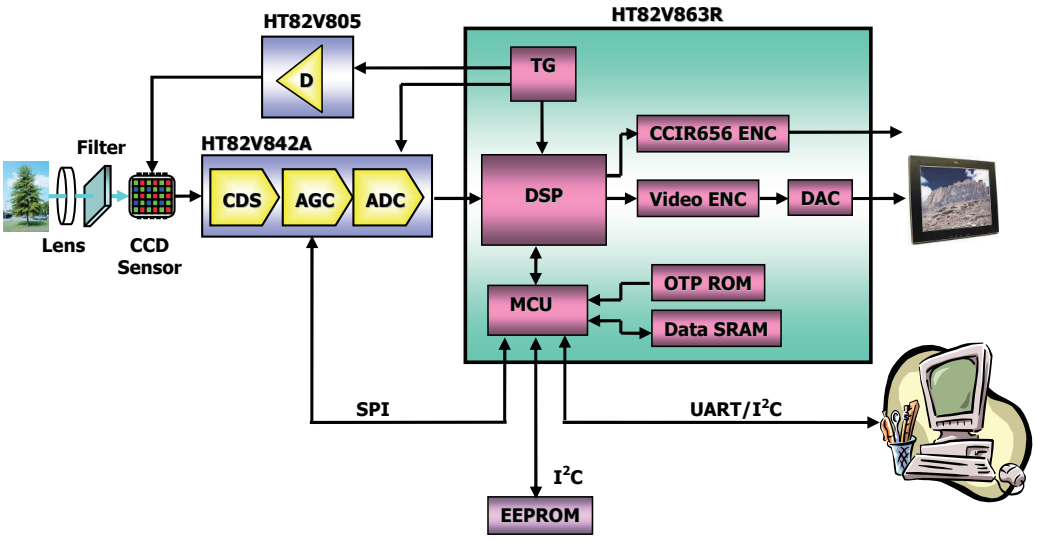
I^2C Interface

The device integrates an OTP ROM for firmware storage. The firmware can be easily programmed into the OTP ROM using the In-System Programming function and the I^2C interface.

Programming Considerations

All configurations in this device are displayed in a user interface window as part of the relevant development tool system. Therefore, the detailed configuration and definitions are not mentioned in this document. Refer to the corresponding user's manual for more detailed configuration information.

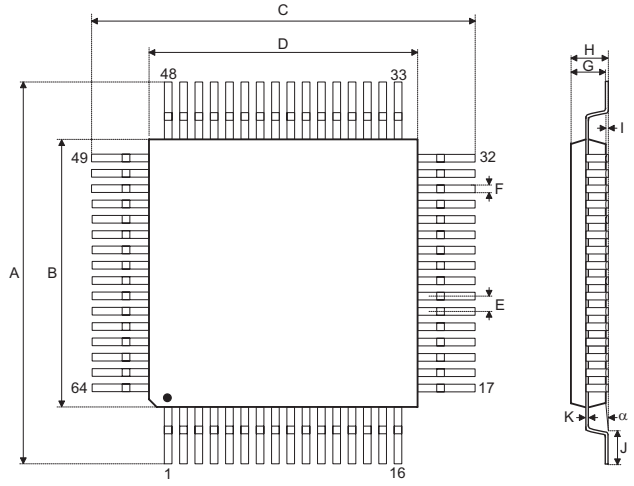
System Application Diagram



Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

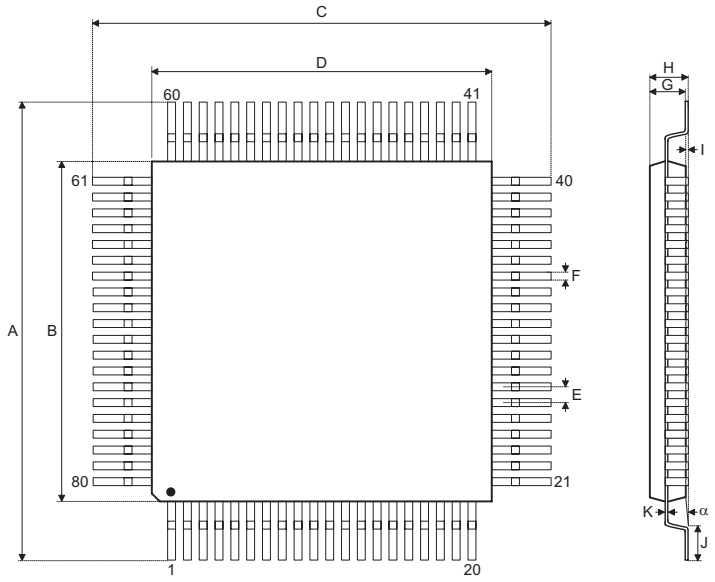
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.016	—
F	0.005	—	0.009
G	0.053	—	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.469	—	0.476
B	0.390	—	0.398
C	0.469	—	0.476
D	0.390	—	0.398
E	—	0.016	—
F	—	0.006	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	11.90	—	12.10
B	9.90	—	10.10
C	11.90	—	12.10
D	9.90	—	10.10
E	—	0.40	—
F	—	0.16	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

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